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Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, April 201(
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. What is meant by a PRAM model ? List and describe the various PRAM models.
2. Distinguish between static and dynamic system interconnection networks. Discuss the benefits and drawbacks of using a digital bus as a dynamic interconnection network.
3. List and explain the four system attributes affecting the performance of the CPU.
4. State Amdahl's Law and describe its significance.
5. Highlight the differences between CISC and RISC processor architectures.
6. Discuss the inclusion, coherence and locality properties of a memory hierarchy.
7. Differentiate between synchronous and asynchronous processor pipeline models. Define the parameters (a) speedup (b) efficiency and (c) throughput in the context of a processor pipeline.
8. Describe the various context switching policies used in multithreaded processor architectures.
9. Discuss the concept of multiport memory as used in a multiprocessor system.
10. Distinguish between static and dynamic data flow computers. **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **any one full** question from **each** Module.

Module – I

11. a) Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment :

Instruction type	CPI	Instruction Mix
Integer arithmetic	1	60%
Data transfer	2	18%
Floating point	4	12%
Control transfer	8	10%

i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

ii) Calculate the corresponding MIPS rate based on the CPI obtained in part (a).

iii) Find the execution time of the object code on this processor. 8

b) Differentiate between multiprocessors and multicomputers. Describe the various multiprocessor and multicomputer architectures in detail. 12

OR

12. a) Write detailed notes on the structure and functioning of vector supercomputers. 10

b) List and explain the Bernstein's conditions for parallel execution of processes. Use the same to identify the portions of the code segment given below that can be executed in parallel and the portions that need to be executed sequentially. Consider each statement as a separate process. Draw the corresponding dependence graph also.

S1 : A = B + C

S2 : C = D × E

S3 : F = G + E

S4 : C = A – F

S5 : M = G + C

S6 : B = L/C

S7 : A = E + B. 10

Module – II

13. a) Describe the structure of a superscalar pipeline in detail. Discuss the various instruction issue and completion policies in superscalar processors. 10

    b) Explain how interleaving can improve the performance of shared memories. Describe the structure of high order interleaved and low order interleaved memory organizations. 10

OR

14. Consider the five staged pipeline processor specified by the following reservation table :

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

a) List the set of forbidden latencies and collision vector.
b) Draw a state diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.
c) List all the simple cycles from the state diagram.
d) Identify the greedy cycles among the simple cycles.
e) What is the Minimum Average Latency (MAL) of this pipeline ?
f) What is the minimum allowed constant cycle in using this pipeline ?
g) What will be the maximum throughput of this pipeline ?
h) What will be the throughput if the minimum constant throughput is used ? 20

Module – III

15. Describe the snoopy bus protocols used to ensure cache coherence in multiprocessor systems. 20

OR

16. a) Write detailed notes on the architecture of the Intel Paragon multicomputer. 12

    b) What is meant by vector processing ? Describe the various possible types of vector instructions in detail. 8